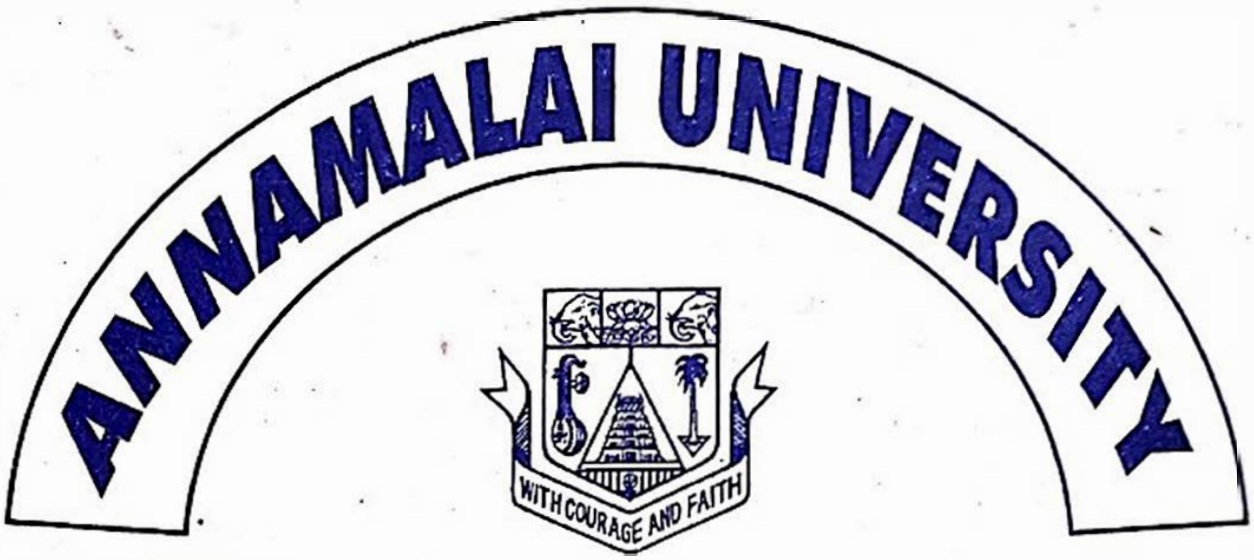



# FACULTY OF ENGINEERING AND TECHNOLOGY

## DEPARTMENT OF ELECTRICAL ENGINEERING

III SEM B.E. ELECTRICAL & ELECTRONICS

## EECP309: ELECTRONIC CIRCUITS SIMULATION LAB

Name .....

Reg. No. .....Batch .....

Class .....

# DEPARTMENT OF ELECTRICAL ENGINEERING

## VISION

To develop the Department into a “Centre of Excellence” with a perspective to provide quality education and skill-based training with state-of-the-art technologies to the students, thereby enabling them to become achievers and contributors to the industry, society and nation together with a sense of commitment to the profession.

## MISSION

M1: To impart quality education in tune with emerging technological developments in the field of Electrical and Electronics Engineering.

M2: To provide practical hands-on-training with a view to understand the theoretical concepts and latest technological developments.

M3: To produce employable and self-employable graduates.

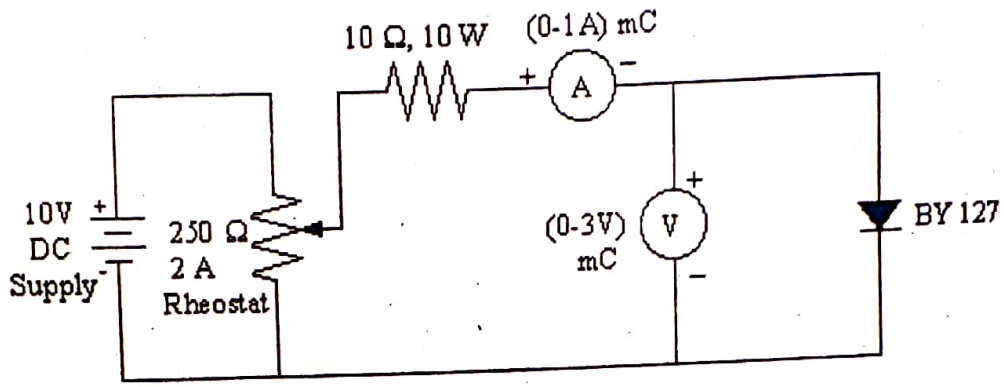
M4: To nurture the personality traits among the students in different dimensions emphasizing the ethical values and to address the diversified societal needs of the Nation

M5: To create futuristic ambience with the state-of-the-art facilities for pursuing research.

# EECP309: ELECTRONIC CIRCUITS SIMULATION LAB

| Sl.No. | Date | Name of the Experiments | Page No. | Marks | Signature |
|---|---|---|---|---|---|
| 1 | | Characteristics of Junction diode, Characteristics of Zener diode and Zener diode as a voltage regulator. | | | |
| 2 | | Half wave and full wave rectifiers with capacitor filter. | | | |
| 3 | | Characteristics of Transistors. | | | |
| 4 | | Characteristics of Field Effect Transistor. | | | |
| 5 | | Zero crossing detector and Schmitt trigger using OP-AMP | | | |
| 6 | | R.C Phase Shift Oscillator using OP-AMP | | | |
| 7 | | Voltage to Current Converter and Current to Voltage Converter | | | |
| 8 | | Instrumentation Amplifier | | | |
| 9 | | Design of Low Pass Filters | | | |
| 10 | | Design of High Pass Filters. | | | |

**Circuit diagram**



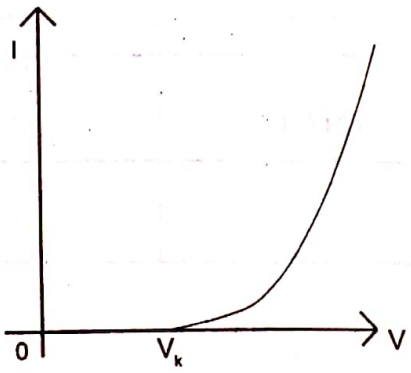

**Design**

Let V = 10V, $I_f$ = 1A

Current limiting resistance $R_{series} = \frac{V}{I_{f_{max}}} = \frac{10}{1} = 10\,\Omega$

Power rating of $R_{series} = I^2R = 1^2 \times 10 = 10\text{W}$

Model Graph



Exp. No.:
Date :

# 5. CHARACTERISTICS OF JUNCTION DIODE

## Aim

To draw the forward characteristics of the given junction diode.

## Theory

Forward biasing

When the external voltage applied to the junction is in such a direction that it cancels the potential barrier, thus permitting current flow, it is called forward biasing.

1. The potential barrier is reduced and at some forward voltage (0.3 to 0.7 V), it is eliminated altogether.
2. The junction offers low resistance (called forward resistance, $R_f$) to current flow.
3. Current flows in the circuit due to the establishment of on the applied forward voltage.

Reverse biasing

When the external voltage applied to the junction is in such a direction that potential barrier is increased, it is called reverse biasing.

1. The junction offers very high resistance (called reverse resistance Rr) to current flow.
2. No current flows in the circuit due to the establishment of high resistance path.

## Apparatus required

| | |
|---|---|
| Ammeter (0-1A) mC | - 1 No |
| DC Regulated power supply (0-30V) | - 1 No |
| Junction diode BY127 | - 1 No |
| Resistor 10Ω, 10W | - 1 No |
| Rheostat 250Ω, 2A | - 1 No |
| Voltmeter (0-3V) mC | - 1 No |

## Specifications

BY 127

| | |
|---|---|
| PIV | 1250 V |
| $I_{F(av)}$ | 1 A |

**Tabulation**

| S. No. | Voltmeter reading V | Ammeter reading mA |
|---|---|---|
| | | |

## Precautions

1. The potential divider must be kept in minimum potential position at the time of starting the experiment.
2. Before starting the experiment the polarities of the diode should be checked.
3. None of the ratings of the device used (BY 127) should be exceeded.

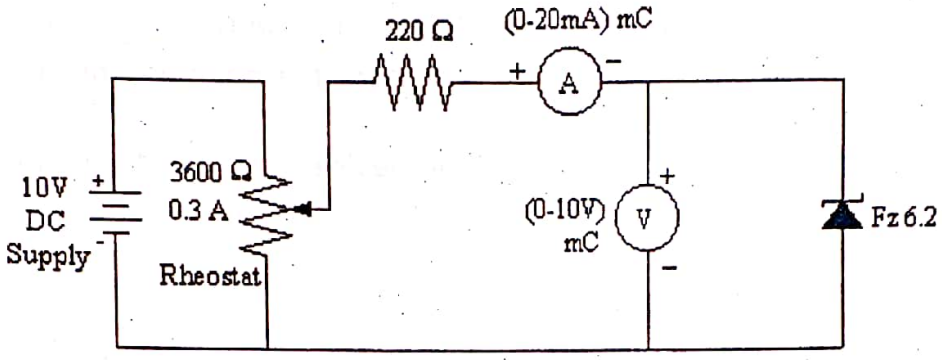
## Procedure

1. The connections are given as per the circuit diagram.
2. Observing the precautions the power supply is switched ON.
3. The potential divider is gradually varied and the corresponding voltmeter, ammeter readings are noted.
4. A graph $I_A$ vs. $V_{AK}$ is plotted.

## Result

The forward bias characteristic of the junction diode is obtained.

**Circuit diagram**



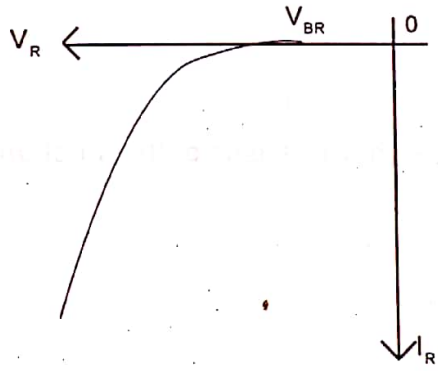

**Design**

Let V = 10V, $V_z$ = 6.2V, $I_T$ = 20 mA

Current limiting resistance $R_{series} = \frac{V - V_Z}{I_T} = \frac{10 - 6.2}{20 \times 10^{-3}} \approx 220\,\Omega$

Power rating of $R_{series} = I^2R = (20 \times 10^{-3})^2 \times 220 = 0.088\text{W}$

Model Graph



# CHARACTERISTICS OF ZENER DIODE

## Aim

To draw the characteristic of the given zener diode.

## Theory

A properly doped crystal diode that has a sharp breakdown voltage is known as zener diode.

1. A zener diode is like an ordinary diode except that it is properly doped so as to have a sharp breakdown voltage.
2. A zener diode is always used in reverse bias condition.
3. If the reverse current is not limited to a safe value in the breakdown region, the zener diode will be burnt out. So, an external resistance is usually connected in the zener diode circuit to limit the reverse current to less than test current.

## Apparatus required

| | |
|---|---|
| Ammeter (0-20mA) mC | - 1 No. |
| DC Regulated power supply (0-30V) | - 1 No. |
| Resistor 220Ω | - 1 No. |
| Rheostat 3600Ω, 0.3A | - 1 No. |
| Voltmeter (0-10V) mC | - 1 No. |
| Zener diode, Fz6.2 | - 1 No. |

## Specifications

Fz 6.2

| | |
|---|---|
| Nominal zener voltage at $I_z$ | 6.2 V |
| Test current, $I_T$ | 20 mA |

## Precautions

1. The potential divider must be kept in minimum potential position at the time of starting the experiment.
2. Before starting the experiment the polarities of the diode should be checked.
3. None of the ratings of the device used (Fz 6.2) should be exceeded.

**Tabulation**

| S. No. | Voltmeter reading V | Ammeter reading mA |
|---|---|---|
| | | |

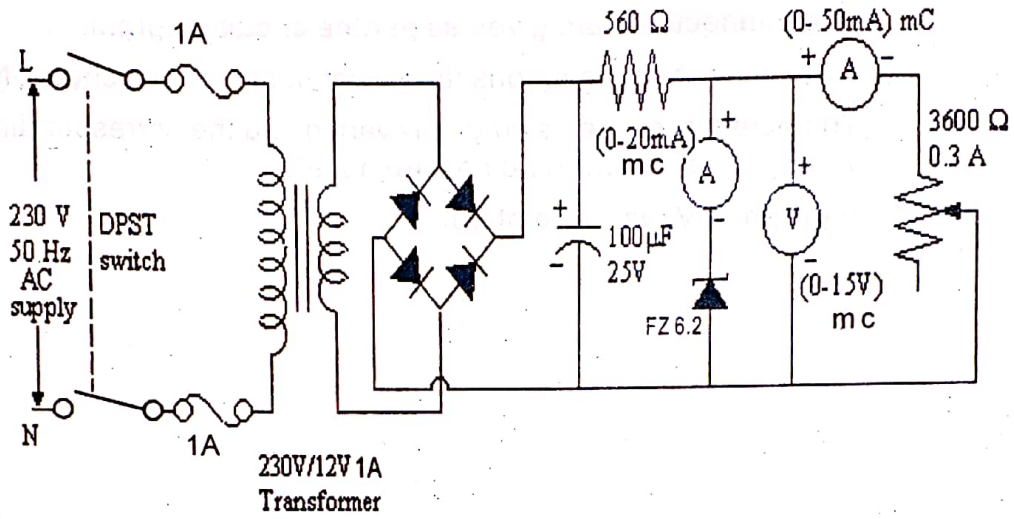
## Procedure

1. The connections are given as per the circuit diagram.
2. Observing the precautions the power supply is switched ON.
3. The potential divider is gradually varied and the corresponding voltmeter, ammeter readings are noted.
4. A graph of $V_z$ vs $I_z$ is plotted.

## Result

The reverse characteristic of the zener diode is obtained.

## Circuit diagram



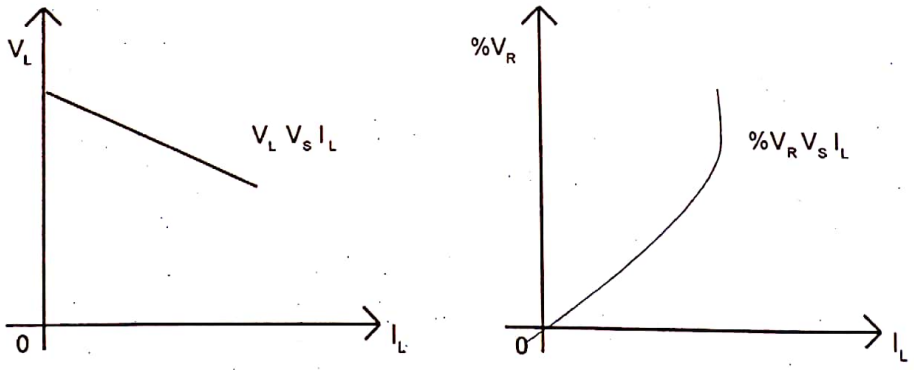

## Design

Let $V_z = 6.2V$, $I_T = 20$ mA

Current limiting resistance $R_{series} = \dfrac{V - V_Z}{I_T} = \dfrac{12\sqrt{2} - 6.2}{20 \times 10^{-3}} \approx 560\,\Omega$

Power rating of $R_{series} = I^2R = \left(20 \times 10^{-3}\right)^2 \times 560 = 0.224\text{W}$

## Model Graph



# ZENER DIODE AS A VOLTAGE REGULATOR

## Aim

To construct a D.C regulated power supply using zener diode and determine its load regulation.

## Theory

In zener diode voltage regulator circuit, the load voltage $V_L$ remains essentially constant (equal to $V_Z$) even though the load resistance $R_L$ may over a wide range. When the input voltage is constant and the load resistance $R_L$ decreases, the load current increases. The extra current cannot come from the source because drop in R will not change as the zener is within its regulating range. The additional load current will come from a decrease in zener current $I_Z$. Consequently, the output voltage stays at constant value.

When $I_Z$ = max, $I_L$ = 0

$I_L$ = max, $I_Z$ = 0

## Apparatus required

Ammeter (0– 50mA) mC - 1 No.
Ammeter (0–25mA)mC - 1 No.
Capacitor 100μF, 25V - 1 No.
Diode 1N 4007 - 4 Nos.
Resistor 560Ω - 1 No.
Rheostat 3600Ω ,0.3 A - 1 No.
Transformer (230/12V) - 1 No.
Voltmeter (0–15V) mC - 1 No.
Zener diode FZ 6.2 - 1 No.

## Specifications:

FZ 6.2

| | |
|---|---|
| Nominal zener voltage at $I_Z$ | 6.2 V |
| Test current, $I_T$ | 20 mA |

## Precautions

1. Zener diode must be reverse biased.
2. The load rheostat must be kept at maximum resistance position, at the time of starting the experiment.
3. The ratings of the devices used should not be exceeded.

**Tabulation**

$V_{NL}$ = V

| S.No. | $I_z$ mA | $I_L$ mA | $V_z$ V | % Voltage Regulation |
|---|---|---|---|---|
| | | | | |

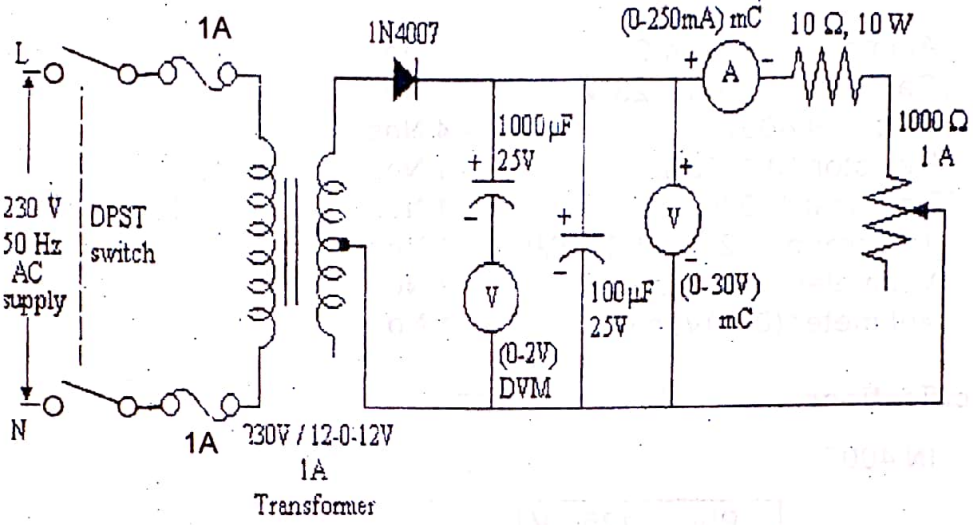
## Procedure

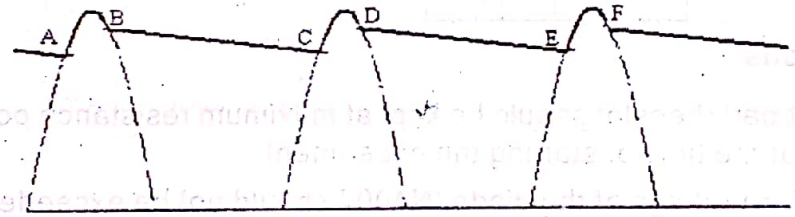
1. Connections are given as per the circuit diagram.
2. The load rheostat is adjusted for different values of load current and the corresponding voltmeter and ammeter readings are noted.
3. The curves $I_L$ vs $V_Z$ & $I_L$ vs % load regulation are plotted.

## Result

The characteristics of zener diode as a voltage regulator are obtained.

## Circuit diagram




## Tabulation

$V_{NL}$ = V

| S. No. | $I_{dc}$ mA | $V_{dc}$ volts | $V_{ac}$ volts | $\%\gamma = \frac{V_{ac}}{V_{dc}} \times 100$ | $\%V_r = \frac{V_{NL} - V_L}{V_{NL}} \times 100$ |
|---|---|---|---|---|---|
| | | | | | |

Exp. No. :
Date :

# 7. HALF WAVE AND FULL WAVE RECTIFIERS WITH CAPACITOR FILTER

## Aim

To construct half wave, full wave and full wave bridge rectifiers using IN4007 semiconductor diode and find its performance characteristics.

## Theory

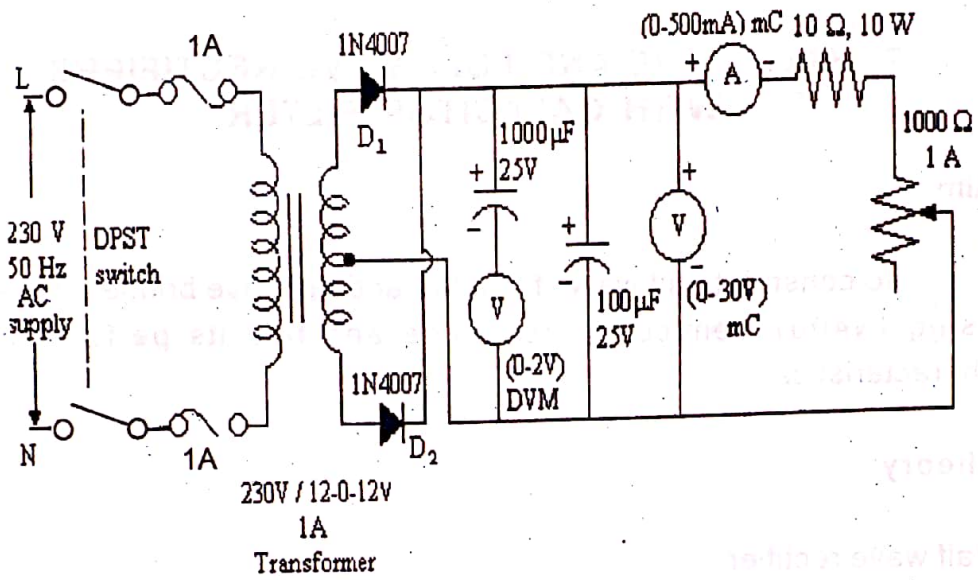
Half wave rectifier

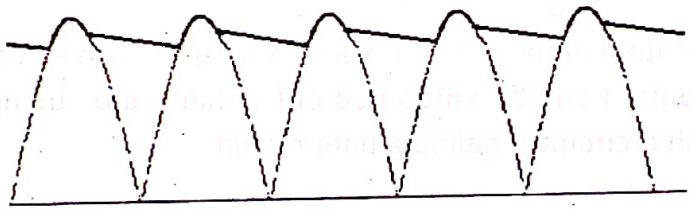
The output of the rectifier is a pulsating dc. The ac component of a rectifier output can be smoothed out or filtered by using a suitable circuit. Such a circuit is called a filter circuit.

The figure shows a half wave rectifier circuit with a single capacitor filter. During the positive half of the input the capacitor gets charged in the time interval between A and B. When the supply ac voltage falls below the dc voltage on the capacitor (at the point B in the figure), the diode ceases to charge the capacitor. But the load current continues because the filter capacitor discharges through the load. This discharge continues up to the point C when the increasing supply voltage exceeds the capacitor voltage. The capacitor then starts charging. The above process repeats. The peak inverse voltage is nearly double the peak voltage $V_m$ of the ac supply.

The load voltage falls from B to C and again D to E and so on at a rate determined by the time constant of the load resistance $R_L$ and filter capacitance C i.e. by $CR_L$. The diode recharges the capacitor from the point A to B, from C to D and so on. The load voltage waveform is therefore the line ABCDEF.

## Circuit diagram



## Tabulation

$V_{NL}$ = V

| S. No. | $I_{dc}$ mA | $V_{dc}$ volts | $V_{ac}$ volts | $\%\gamma = \frac{V_{ac}}{V_{dc}} \times 100$ | $\%V_r = \frac{V_{NL} - V_L}{V_{NL}} \times 100$ |
|---|---|---|---|---|---|
| | | | | | |

Full wave rectifier

A change over from a half wave to full wave rectifier gives rise to the following changes.

i. The dc load voltage shifts only slightly towards the limiting value Vm.
ii. The peak-to-peak ripple voltage gets halfed.
iii. The frequency of the ripple voltage gets doubled.
iv. The individual diode current gets halfed.
v. There is no change in PIV.

**Apparatus required**

| | |
|---|---|
| Ammeter (0-1A) mC | - 1 No. |
| Capacitor 100μF, 25V | - 1 No. |
| Capacitor 1000μF, 25V | - 1 No. |
| Digital voltmeter (0-2V) | - 1 No. |
| Diode IN 4007 | - 4 Nos. |
| Resistor 10Ω, 10W | - 1 No. |
| Rheostat 1000Ω, 1A | - 1 No. |
| Transformer 230V / 12-0-12V | - 1 No. |
| Voltmeter (0-30V)mC | - 1 No. |

**Specifications**

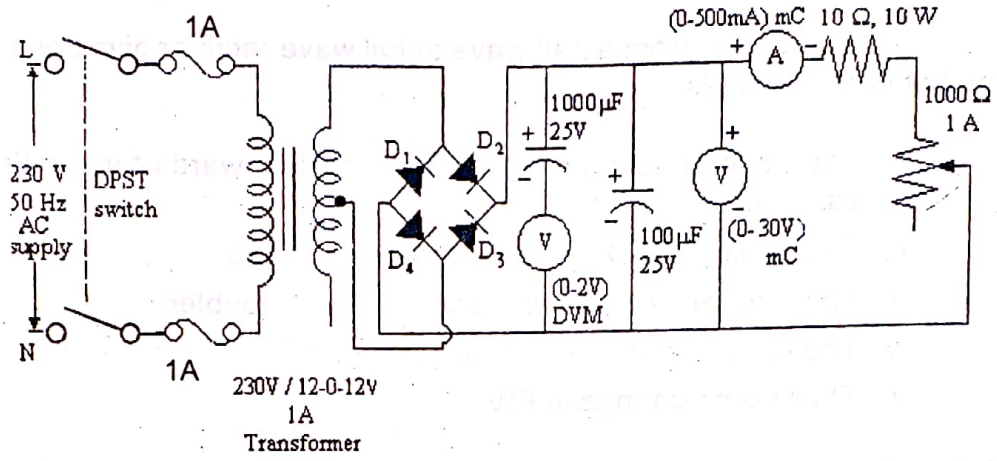
IN4007

| | |
|---|---|
| PIV | 1250 V |
| $I_{F(av)}$ | 1 A |

**Precautions**

1. Load rheostat should be kept at maximum resistance position at the time of starting the experiment.
2. The polarities of the electrolytic capacitors should be properly checked before switching on the supply.
3. Ranges and polarities of the meters are checked and connected properly.
4. The ratings of the devices used should not be exceeded.

## Circuit diagram




## Tabulation

$V_{NL}$ = V

| S. No. | $I_{dc}$ mA | $V_{dc}$ volts | $V_{ac}$ volts | $\%\gamma = \frac{V_{ac}}{V_{dc}} \times 100$ | $\%\ V_r = \frac{V_{NL} - V_L}{V_{NL}} \times 100$ |
|---|---|---|---|---|---|
| | | | | | |

## Procedure

1. Connections are made as per the circuit diagram.
2. Observing the precautions the power supply is switched ON.
3. The no-load readings are noted.
4. The load current is increased in steps and for each step the other meter readings are noted and tabulated.

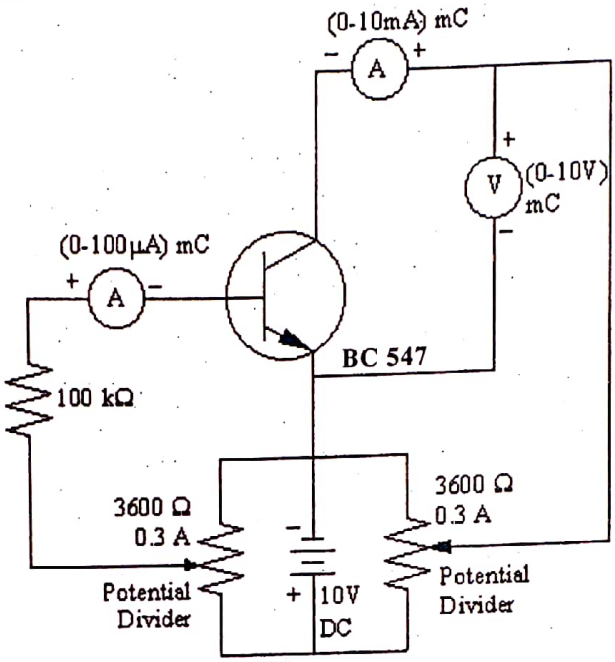
## Graph

The curves $I_{dc}$ vs $V_{dc,}$ $I_{dc}$ vs % $\gamma$ and $I_{dc}$ vs % $V_r$ for half wave, full wave and bridge rectifiers are plotted.

## Result

The performance curves of half wave, full wave and bridge rectifiers with capacitor filter are plotted.

Circuit diagram




**Tabulation**

| $I_B$ = 10 μA | | $I_B$ = 20 μA | | $I_B$ = 30 μA | |
|---|---|---|---|---|---|
| $V_{CE}$ volts | $I_C$ mA | $V_{CE}$ volts | $I_C$ mA | $V_{CE}$ volts | $I_C$ mA |
| | | | | | |

Exp. No.:
Date :

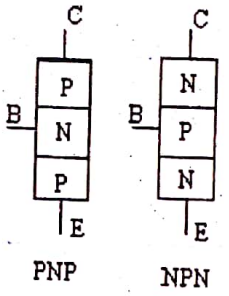
# 1. CHARACTERISTICS OF TRANSISTORS

## Aim

To plot and study the output characteristics of given NPN and PNP transistors.

## Theory

The transistor consists of two back PN junctions manufactured in a single piece of semiconductor crystal. These two junctions give rise to three regions called emitter, base and collector.




The Figure 1 shows a layer of N-type material sandwiched between two layers of p-type material. It is described as PNP transistor. Figure 2 shows an NPN transistor consisting of a layer of p-type material sandwiched between two layers of N -type material.

### Emitter

The section on one side that supplies charge carriers (either electrons or holes) is called the emitter. It is heavily doped than any of the other regions.

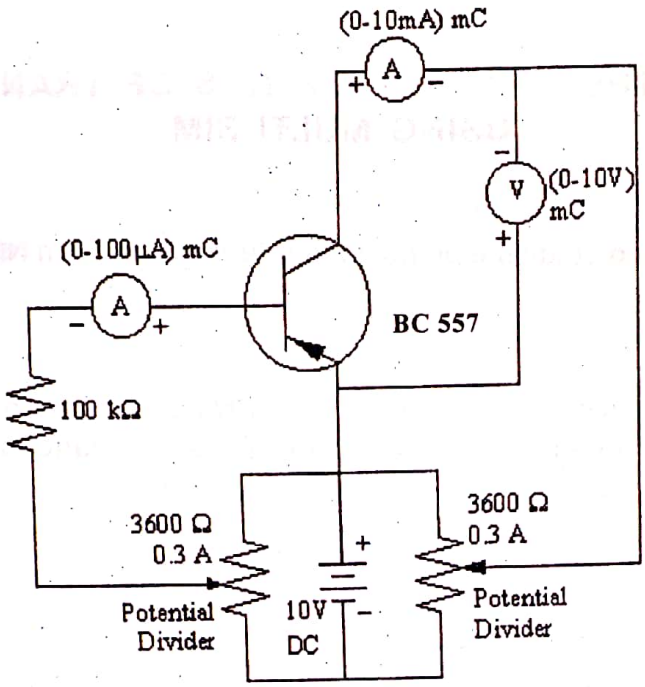
### Collector

The section on the other side that collects the charge carriers is called the collector, which is moderately doped.

### Base

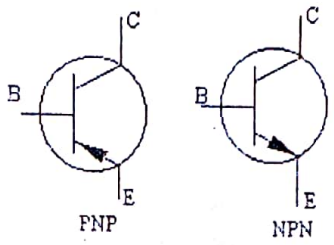
The middle section that forms two PN junctions between the emitter and collector is called the base. It is very thin as compared to either the emitter or the collector and is very lightly doped.

## Circuit diagram




## Tabulation

| $I_B$ = 10 μA | | $I_B$ = 20 μA | | $I_B$ = 30 μA | |
|---|---|---|---|---|---|
| $V_{CE}$ volts | $I_C$ mA | $V_{CE}$ volts | $I_C$ mA | $V_{CE}$ volts | $I_C$ mA |
| | | | | | |




The emitter, base and collector are provided with terminals, which are labeled as E, B and C. The figure shows the symbolic representation of PNP and NPN transistors. The arrowhead is always at the emitter and in each case, its direction indicates the conventional direction of current flow.

The base emitter junction is forward biased, allowing low resistance for the emitter circuit. The base-collector junction is reverse biased and provides high resistance in the collector circuit. The transistor can perform a number of functions but the most important of them is its amplifying action. A weak signal is introduced in the low resistance circuit and amplified output is taken from the high resistance circuit. Therefore, a transistor transfers a signal from a low resistance to a high resistance. Prefix "trans" means the signal transfer property of the device while "istor" classifies it as a solid element in the family of resistors.

**Apparatus required**

| | |
|---|---|
| Ammeter (0–100mA) mC | - 1 No. |
| Ammeter (0–100μA) mC | - 1 No. |
| DC Regulated power supply (0 –30V), 2A | - 1 No. |
| Resistor 100 kΩ | - 1 No. |
| Rheostat 3600 Ω, 0.3A | - 2 Nos. |
| Transistors SK 100, SL 100 | - 1 each |
| Voltmeter (0–10V) mC | - 1 No. |
| Ammeter (0–10mA) mC | - 1 No. |

**Specifications**

SL100 -Absolute Maximum ratings

| | |
|---|---|
| $V_{CBO}$ | 60V |
| $V_{CEO}$ | 50V |
| $V_{BEO}$ | 6V |
| $I_C$ | 500 mA |
| $h_{FE}$ | 40/300 at $V_{CE}$ = 5V $I_C$ = 0.5 A |

## Design

$$\beta = \frac{I_C}{I_B}$$

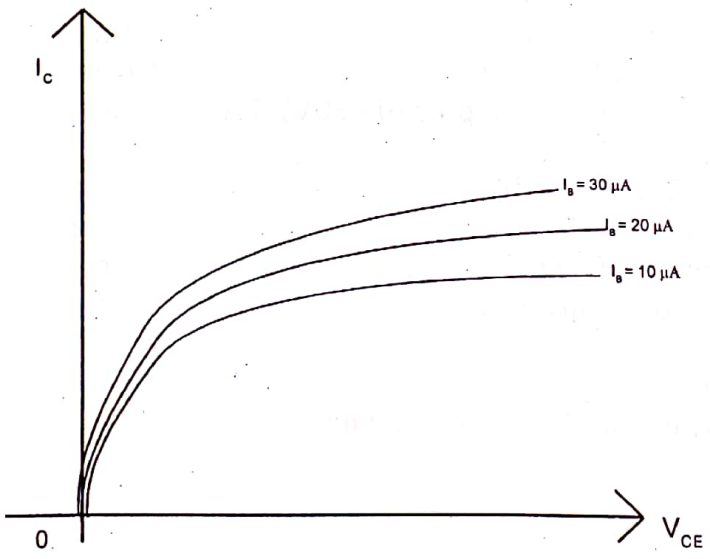
Assuming $I_C = 10\text{mA}$

choosing $\beta = 100$

$$I_B = \frac{I_C}{\beta} = \frac{10\times10-3}{100} = 0.1\,\text{mA}$$

$$\text{Base resistance } R_{BB} = \frac{V_{BB_{max}}}{I_B} = \frac{10}{0.1\times10^{-3}} = 100\,\text{k}\Omega$$

Model Graph



SK 100 - TO 5 package - PNP

| | |
|---|---|
| $V_{CBO}$ | 60V |
| $V_{CEO}$ | 50V |
| $V_{BEO}$ | 6V |
| $I_C$ | 500 mA |
| $h_{FE}$ | 40/300 at $V_{CE} = 5V$ $I_C = 100$ mA |

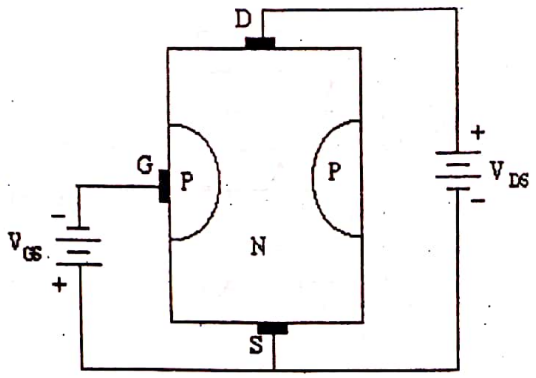
## Procedure

1. Fabricate the circuits using multisim as per the circuit diagram.
2. The base current $I_B$ is kept constant, the collector to emitter voltage is varied in steps, and the corresponding collector current is noted down.
3. The above procedure is repeated for different values of base current.
4. The curves of $I_C$ vs. $V_{CE}$ are plotted for different values of $I_B$.

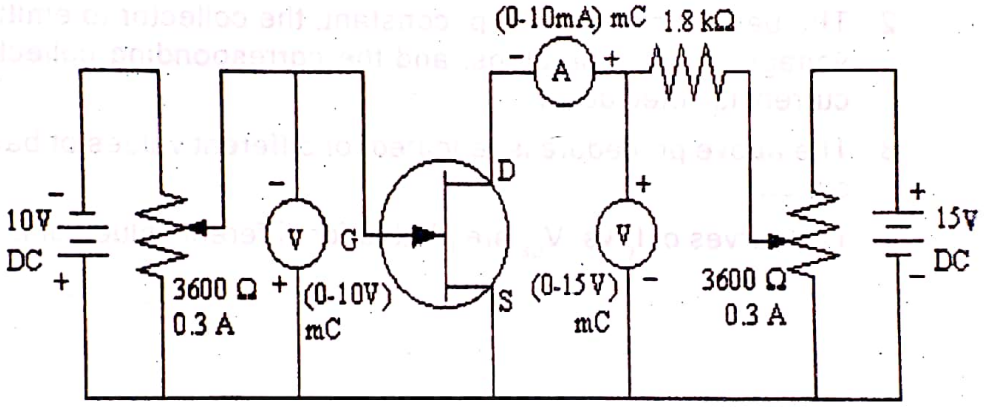
## Result

The characteristics of NPN and PNP transistors have been plotted and studied.

## FET




## Circuit diagram



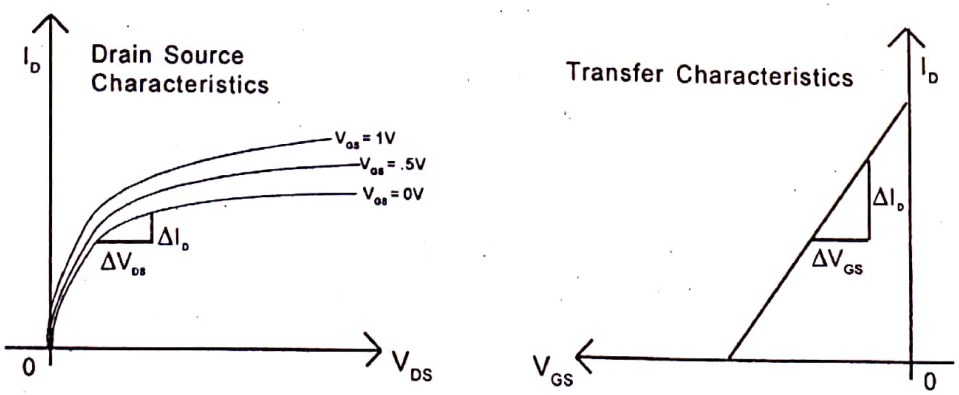

## Design

$$I_{Dmax} = 8mA$$

$$V_{DSmax} = 15V$$

$$R = \frac{V_{DS}}{I_D} = \frac{15}{8\times10^{-3}} = 1.8k\Omega$$

## Model Graph



Exp. No. :
Date :

## 2. CHARACTERISTICS OF FIELD EFFECT TRANSISTOR

### Aim

To plot and study the characteristics of a given field effect transistor.

### Theory

When a voltage $V_{GS}$ is applied between drain and source terminals with gate voltage $V_{GS}$ = 0V, the two PN junctions at the sides of the bar establish very thin depletion layers. The electrons will flow from source to drain through a channel between the depletion layers. The size of these layers determines the width of the channel and hence the current through the channel is maximum and this current is designated as $I_{DSS}$.

When a reverse voltage $V_{GS}$ is applied between the gate and source, the width of the depletion layer increases. This reduces the width of the conducting channel, thereby increasing the resistance of N type silicon bar. Consequently the current from source to drain decreases. On the other hand, if the reverse voltage on the gate is decreased, the width of the depletion layer also decreases. This increases the width of the conducting channel and hence source to drain current.

It is clear from the above discussion that source to drain current can be controlled by the application of electric field (potential) on the gate. For this reason, the device is called field effect transistor.

### Apparatus required

| | |
|---|---|
| Ammeter (0- 10 mA) mC | - 1 No. |
| DC Regulated power supply (0-30V), 2A | - 2 Nos. |
| FET - BFW 10 | - 1 No. |
| Resistor 1.8 kΩ | - 1 No. |
| Rheostat 3600 Ω, 0.3A | - 2 Nos. |
| Voltmeter (0- 15V) mC | - 2 Nos. |

### Specifications

BFW 10 - FET

| | |
|---|---|
| $V_{DS}$ | 30 V |
| $-V_{GSO}$ | 30 V |
| $P_{tot}$ | 300 mW |
| $I_{Dmax}$ | 8 mA |

**Tabulation**

| S. No. | $V_{GS}$ = 0V | | $V_{GS}$ = V | | $V_{GS}$ = V | | $V_{GS}$ = V | | $V_{GS}$ = V | |
|---|---|---|---|---|---|---|---|---|---|---|
| | $V_{DS}$ V | $I_D$ mA | $V_{DS}$ V | $I_D$ mA | $V_{DS}$ V | $I_D$ mA | $V_{DS}$ V | $I_D$ mA | $V_{DS}$ V | $I_D$ mA |
| | | | | | | | | | | |

**Formulae**

AC drain resistance

$$R_D = \left.\frac{V_{DS}}{I_D}\right|_{\text{at constant } V_{GS}}$$

Trans-conductance

$$G_m = \left.\frac{I_{DS}}{V_{GS}}\right|_{\text{at constant } V_{DS}}$$

Amplification factor

$$\mu = \left.\frac{VDS}{VGS}\right|_{\text{at constant } I_D}$$

$$= G_m \times R_D$$

Transfer Characteristics of FET

| $V_{DS}$ | |
|---|---|
| $V_{GS}$ | $I_{DS}$ |
| | |

**Precautions**

1. The potential divider should be kept at minimum potential position at the time of switching ON the supply.
2. The ratings of the device used should never be exceeded.

**Procedure**

1. Connections are made as per the circuit diagram.
2. The gate to source voltage $V_{GS}$ is kept constant, say zero volts and the drain source voltage $V_{DS}$ is varied in steps and corresponding drain current $I_D$ is noted down.
3. The above procedure is repeated for different values of $V_{GS}$.
4. The curves of $I_D$ vs. $V_{DS}$ are drawn for different values of $V_{GS}$.
5. From the graph find RD, Gm and $\mu$ are found out.

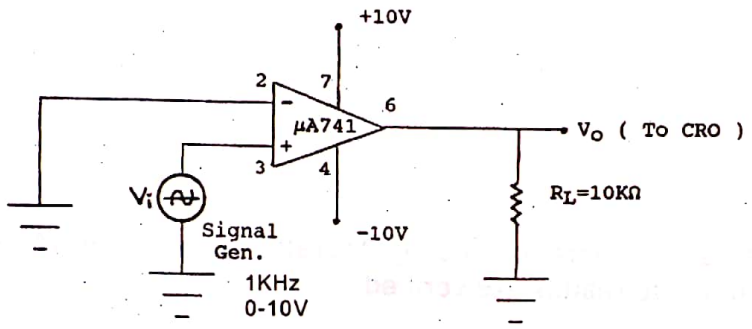
Transfer characteristics of FET

1. In the drain source characteristics, keeping $V_{DS}$ constant, the drain current $I_D$ is noted for different values of $V_{GS}$.
2. The above procedure is repeated for different values of $V_{DS}$.
3. A graph is drawn between gate source voltage $V_{GS}$ and drain current $I_D$.
4. From the graph, the transconductance $G_m$ is found out.

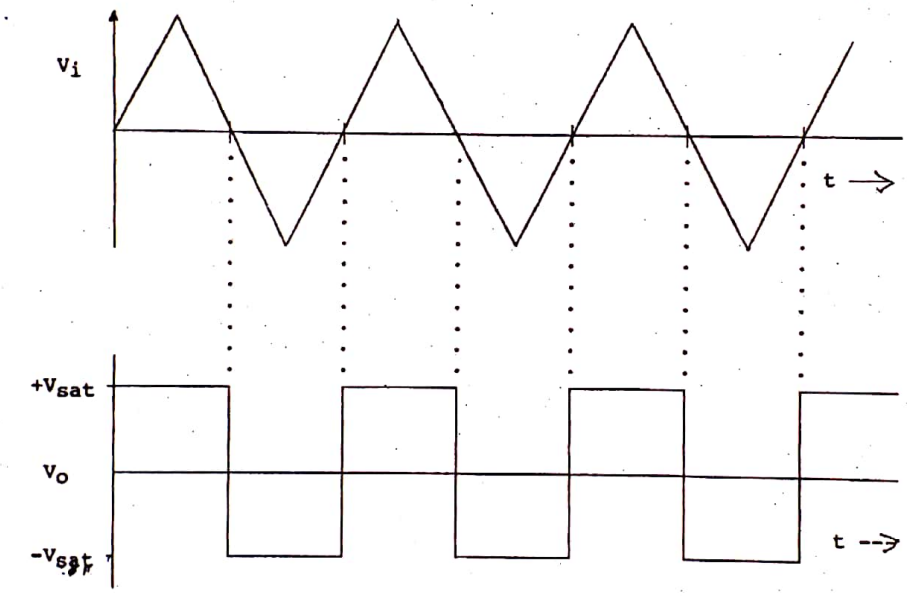
**Result:**

Thus the characteristics of FET are obtained and the parameters of FET are determined experimentally.

## NON-INVERTING ZERO CROSSING DETECTOR




**Model waveform**



Expt No:
Date :

## ZERO CROSSING DETECTOR AND SCHMITT TRIGGER USING OPERATIONAL AMPLIFIERS

**Aim :**

To design and construct

1. Zero Crossing detector and
2. Schmitt trigger using the given operational amplifier μA 741 and to trace both input and output waveforms.

**Apparatus required :**

**Specifications :**

**Theory :**

**Zero Crossing detector :**

There are two types of zero crossing detectors.

1. Non-inverting zero-crossing detector
2. Inverting zero crossing detector.

**Non-inverting zero crossing detector :**

1. In non-inverting zero crossing detector, the input signal $V_i$ is applied to non-inverting input terminal of op-amp and the inverting input terminal is grounded,

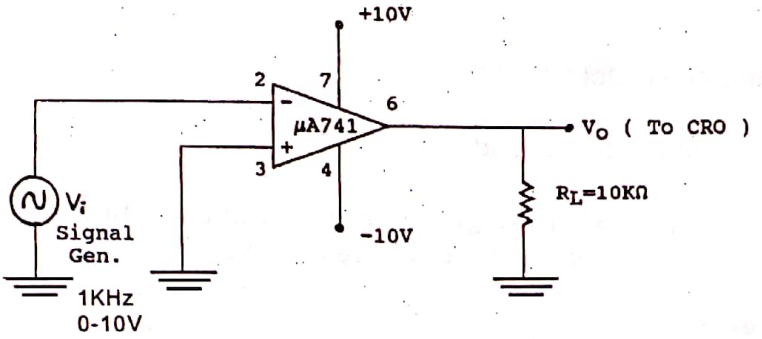
   i.e., $V_{ref} = V_{inv} = 0$

2. The o/p voltage, $V_o$ is given by

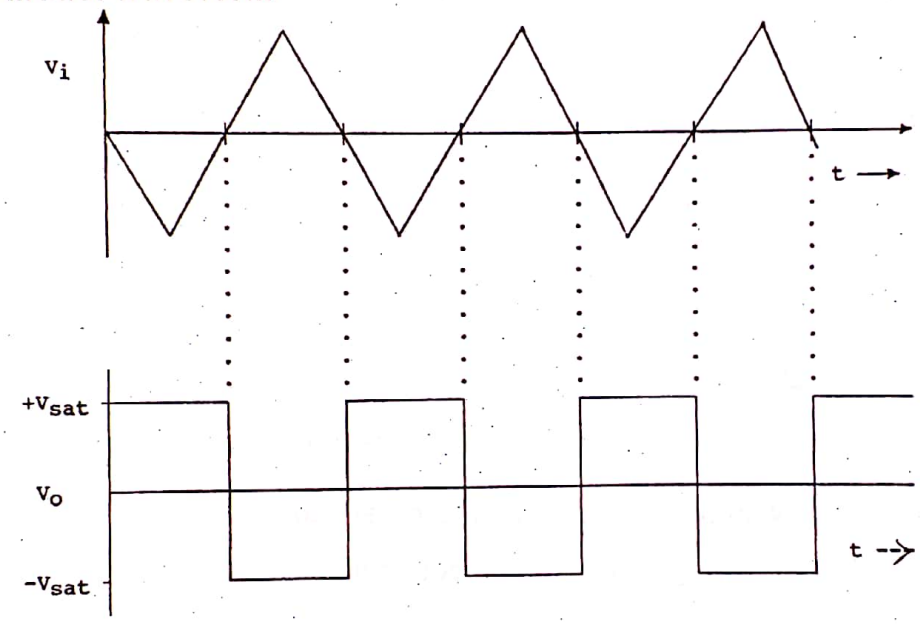
   $$V_o = A_v \cdot V_i$$

   Where $A_v$ = open loop gain of op-AMP.

## INVERTING ZERO CROSSING DETECTOR




**Model waveform**



3. When $V_i$ is slightly greater than zero, the o/p voltage, $V_o$, is driven to +ve saturation '$+V_{sat}$'.

4. When $V_i$ is slightly lower than zero, the o/p is driven to -ve saturation '$-V_{sat}$'

5. When $V_i$ passes through zero in the +ve direction, the o/p voltage $V_o$ is driven into +ve saturation. Conversely, when $V_i$ passes through, zero in the -ve direction, $V_o$ switches and saturates -vely. Thus, in non- inverting zero crossing detector the input signal is amplified by a gain Av and the o/p is inphase with the input signal.

**Inverting zero crossing detector :**

6. In inverting zero crossing detector, the input signal $V_i$ is applied to inverting input of op-amp and the non-inverting input is grounded.

$$\text{i.e., } V_{noninv} = V_{ref} = 0$$

7. The o/p voltage $V_o$ is given by

$$V_o = -A_v.V_i$$

The -ve sign indicates that the o/p is out of phase with respect to input by 180° or is of opposite polarity.

8. When Vi passes through zero in the +ve direction, the o/p $V_o$ is driven into -ve saturation. Conversely, when $V_i$ passes through, zero in the -ve direction, the o/p $V_o$ switches and saturates +vely.

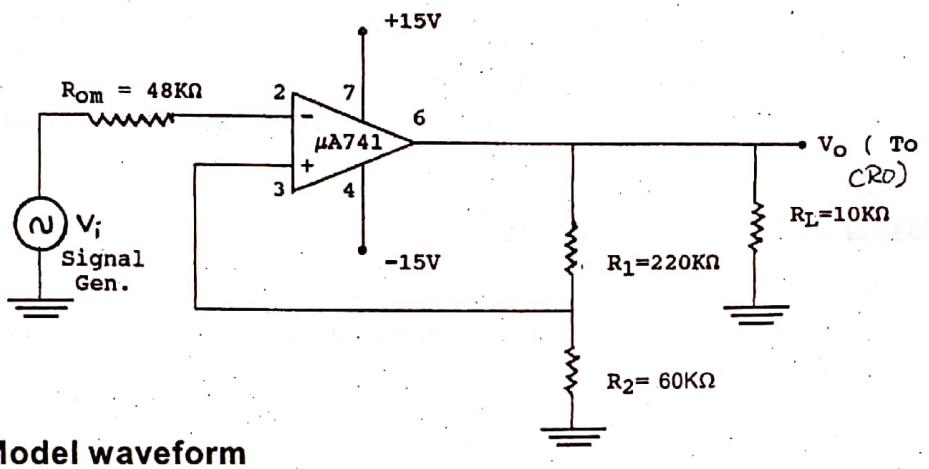
9. Thus, in the inverting zero crossing detector signal is amplified by gain $A_v$ and is also inverted at the o/p.

**Schmitt Trigger :**

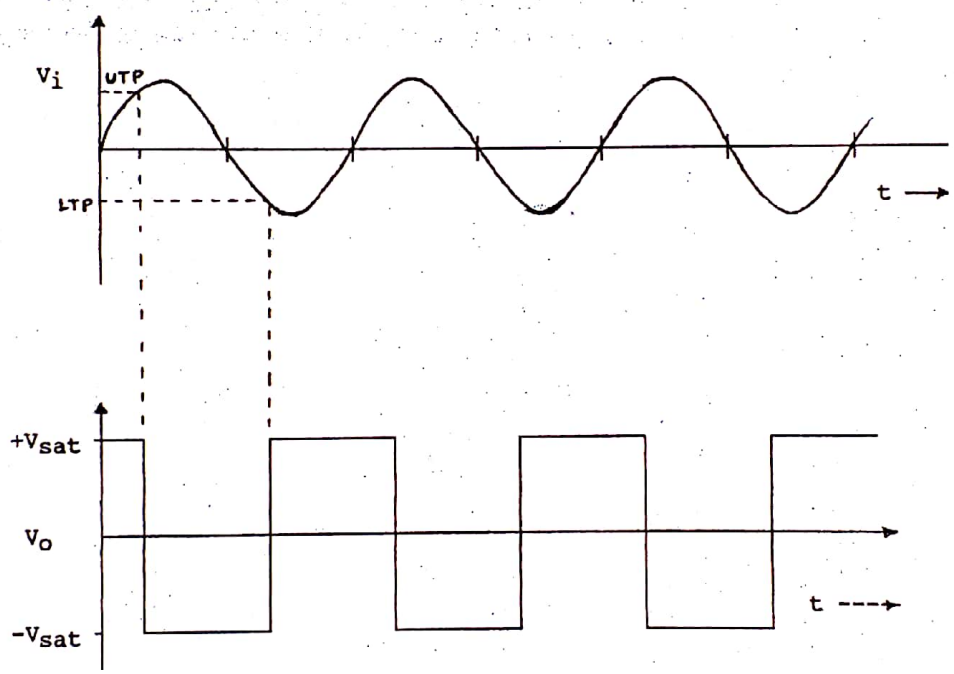
Figure shows an inverting comparator with positive feedback. This circuit converts an irregular-shaped waveform to a square wave or pulse. The circuit is known as the Schmitt trigger or squaring circuit. The input voltage $V_{in}$ triggers (changes the state of) the output Vo every time it exceeds certain voltage levels called the upper threshold voltage $V_{ut}$ and lower threshold voltage $V_{lt}$, as shown in figure.

In figure, these threshold voltages are obtained by using the voltage divider $R_1$ - $R_2$, where the voltage across $R_1$ is fed back to the (+) input. The voltage across $R_1$ is a variable reference threshold voltage that depends on the value and polarity of the output voltage $V_o$. When $V_o = +v_{sat}$, the voltage across $R_1$ is called the upper threshold voltage, $V_{ut}$. The input voltage $V_{in}$ must be slightly more positive than $V_{ut}$ in order to cause the output $V_o$ to switch from $+V_{sat}$ to $-V_{sat}$. As long as $V_{in} < V_{ut}$, Vo is at +Vsat. Using the voltage-divider rule.

## SCHMITT TRIGGER




**Model waveform**



$$V_{ut} = \frac{R_1}{R_1 + R_2} (+V_{sat})$$

On the otherhand, when $V_o = -V_{sat}$, the voltage across $R_1$ is referred to as lower threshold voltage, $V_{lt}$. $V_{in}$ must be slightly more negative than $V_{lt}$ in order to cause $V_o$ to switch from $-V_{sat}$ to $+V_{sat}$. In other words, for $V_{in}$ values greater than $V_{lt}$, $V_o$ is at $-V_{sat}$. $V_{lt}$ is given by the following equation :

$$V_{lt} = \frac{R_1}{R_1 + R_2} (-V_{sat})$$

Thus, if the threshold voltages $V_{ut}$ and $V_{lt}$ are made larger than the input noise voltages, the positive feedback will eliminate the false output transitions. Also, the positive feedback, because of its regenerative action, will make $V_o$ switch faster between $+V_{sat}$ and $-V_{sat}$. In figure, resistance $R_{OM} \approx R_1 \,||\, R_2$ is used to minimize the offset problems.

**Precautions :**

1. None of the ratings should be exceeded.
2. Connections are made with proper polarities.

**Design :**

Let $V_{ut} = V_{lt} = 3V$

$+V_{sat} = +14V$

$-V_{sat} = -14V$

$I_{p.d} = 50\mu A$

$V_{R2} = V_{ut} = I_{p.d} \times R_2$

$$R_2 = \frac{3}{50 \times 10^{-6}} = 60\ K\Omega$$

$$R_1 = \frac{V_o - V_{ut}}{I_{p.d}} = \frac{14-3}{50 \times 10^{-6}} = 220\ K\Omega$$

$R_{OM} = 60\ K\Omega \,||\, 220K\Omega = 47.14\ K\Omega \simeq 48K\Omega$

**Procedure :**

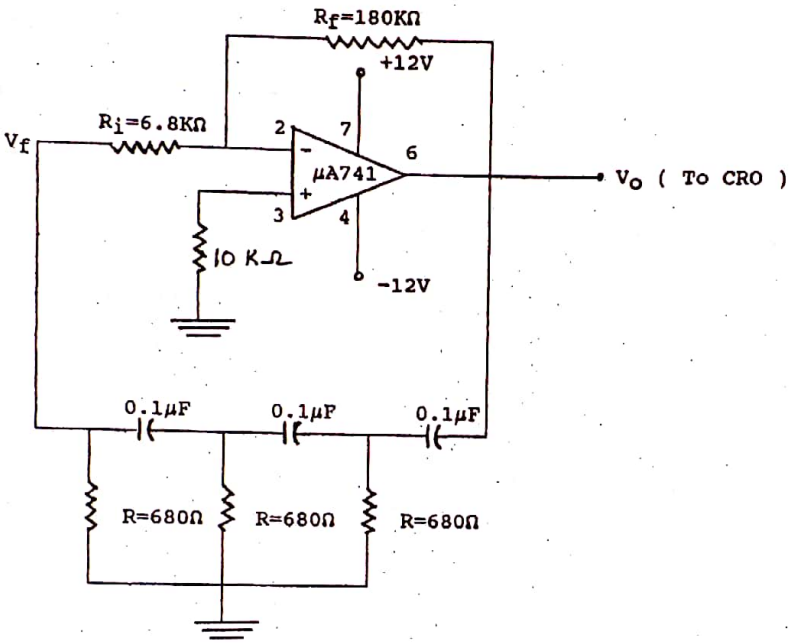
1. The Connections are given as per the circuit diagram.
2. The power supply is switched ON.
3. The input signal is applied.
4. The input as well as output signals are traced.

**Result :**

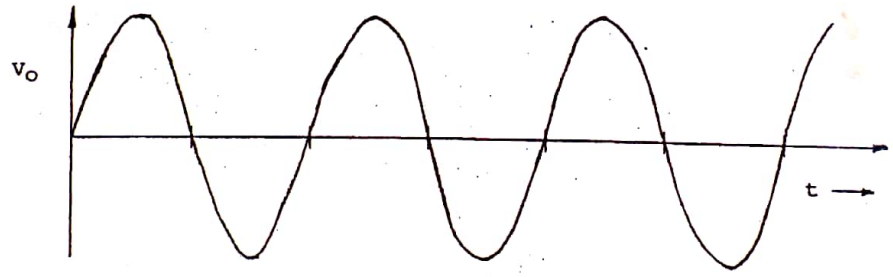
Zero crossing detectors and Schmitt trigger circuits were designed and constructed and output waveforms were traced.

**Questions :**

## RC PHASE SHIFT OSCILLATOR




**Model waveform**



Expt No:
Date :

## RC PHASE SHIFT OSCILLATOR USING OP-AMP

**Aim :**

To design and construct R-C phase shift oscillator using the given op-amp μA 741 and to trace the output waveforms.

**Apparatus required :**

**Specifications :**

**Theory :**

Figure shows a phase shift oscillator. The op-amp provides a phase shift of 180° as it is used in the inverting mode. An additional phase shift of 180° is provided by the feedback RC network. The transfer function of the RC network can be easily calculated as,

$$\beta = \frac{V_f}{V_o} = \frac{1}{1 + 6/sRC + 5/s^2R^2C^2 + 1/s^3R^3C^3}$$

Letting $s = j\omega$,

$$\beta = \frac{1}{1 - 5(f_1/f)^2 - j[6(f_1/f) - (f_1/f)^3]} \quad \text{------(1)}$$

where

$$f_1 = \frac{1}{2\pi RC}$$

For $A_v \beta = 1$, $\beta$ should be real. So the imaginary term in Eqn. (1) must be equal to zero, that is,

$$6(f_1/f) - (f_1/f)^3 = 0$$

or $$f_1/f = \sqrt{6}$$

The frequency of oscillation $f_o$ is given by,

$$fo = \frac{1}{\sqrt{6}(2\pi RC)}$$

Also the loop gain $A_v\beta = 1$

or, $$\frac{A_v}{1 - 5(f_1/f_o)^2} = 1$$

or, $$A_v \geq -29$$

That is the gain of the inverting op-amp should be atleast 29, or $R_f = 29\ R_1$. The gain $A_v$ is kept greater than 29 to ensure that variations in circuit parameters will not make $A_v \beta = 1$, otherwise oscillations will die out.

For low frequencies (less than 1KHz), op-amp μA 741 may be used, however for high frequencies, LM 318 or LF 351 should be used.

**Design :**

Let C = 0.1 μF, F = 1000 Hz

$$R = \frac{1}{\sqrt{6} \times 2\pi \times (0.1 \times 10^{-6}) \times 1000} = 649\Omega$$

To prevent loading of the amplifier by RC network, $R_1 > 10R$

Therefore, let $R_1 = 10R = 10 \times 649 = 6.49\ K\Omega$

since $R_f = 29\ R_1$

$R_f = 29 \times 6.49 = 188.2\ K\Omega$

**Precautions :**

1. None of the ratings should be exceeded.
2. The polarities of power supply should be connected properly to Op-amp.

**Procedure :**

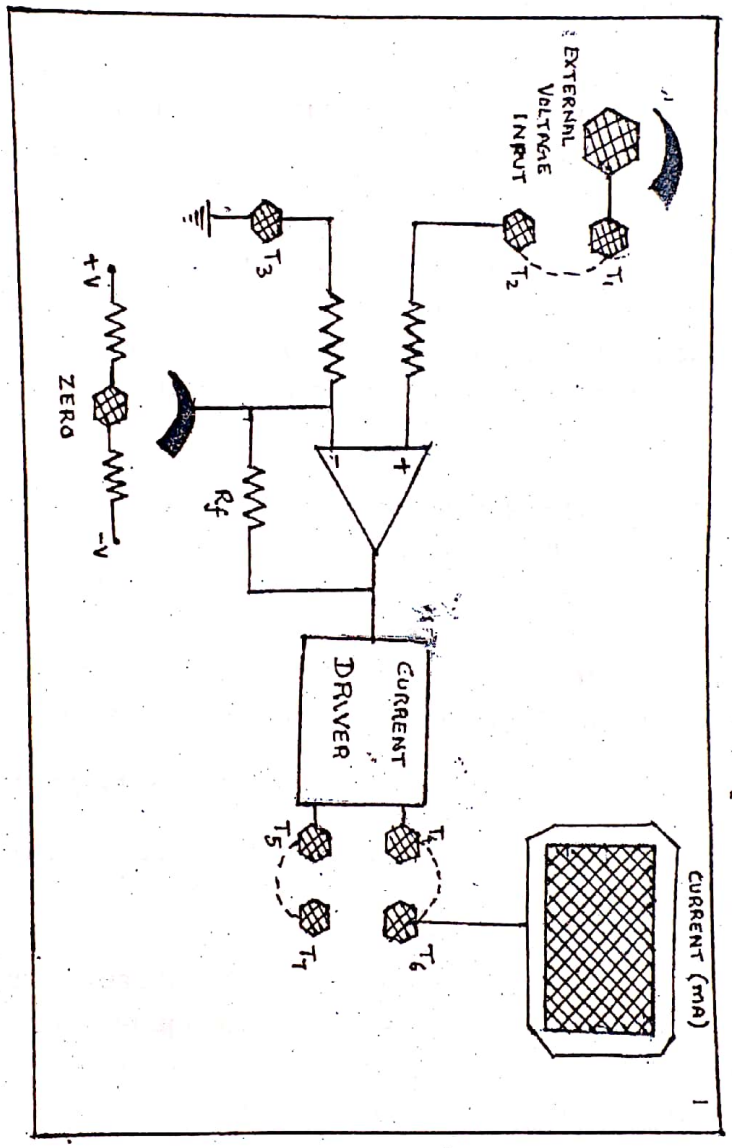
1. The connections are given as per the circuit diagram.
2. The power supply is switched ON.
3. Output waveforms are traced.

**Result :**

RC phase shift oscillator using op-amp μA 741 was designed and constructed and output waveforms were traced.

**Questions :**

# VOLTAGE TO CURRENT CONVERTER MODULE (ITB-11)



Expt No:
Date :

## VOLTAGE TO CURRENT CONVERTER

**Aim**

To study the characteristics of voltage to current converter

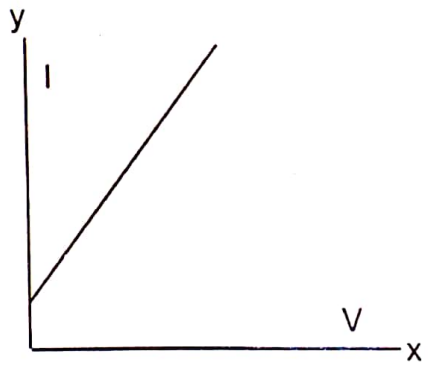
**Apparatus required**

| | |
|---|---|
| Operational Amplifier μA 741 | - 2 Nos |
| Resistors | |
| Voltmeter (0-10v)mc | - 1 No |
| Ammeter (0-20mA) mc | - 1 No |
| D.C. Dual Power Supply | - 1 No |
| D.C. Power Supply | - 1 No |

**Specifications**

| V volts | I mA |
| --- | --- |
| | |

**Model Graph**



**Precautions**

1. The pin numbers should be checked before starting the experiment
2. Loose connections must be avoided.
3. The operational amplifier should be connected with proper polarity and the supply voltage should not exceed $\pm$15 V.

**Procedure**

1. Connections are made as given in the circuit diagram
2. The input voltage is varied from 0 to 10V in steps and the corresponding output currents are noted from the ammeter
3. A graph is drawn between the voltage and current.

**Result**

Thus characteristics of voltage to current converter was studied.

## CURRENT TO VOLTAGE CONVERTER

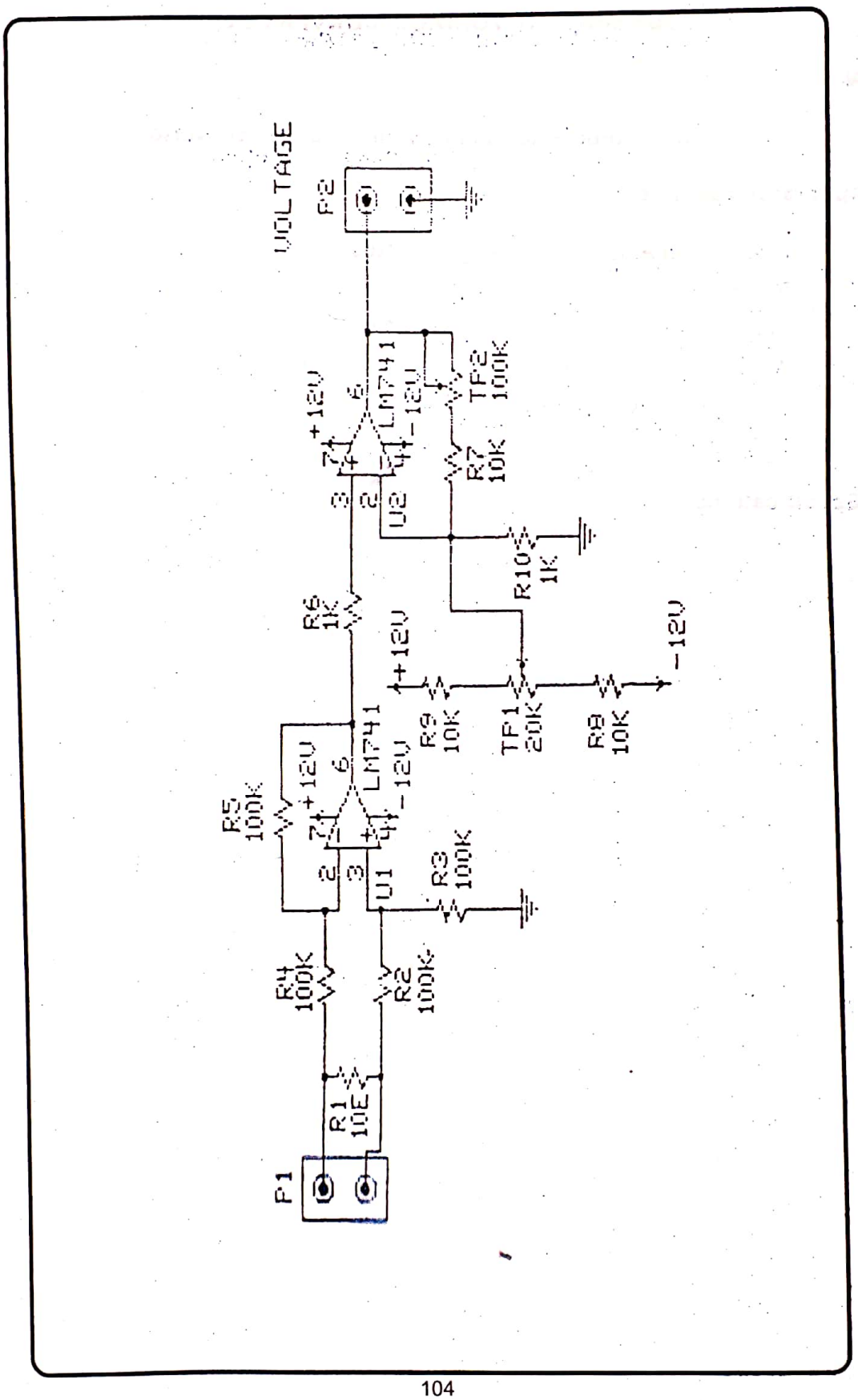
**Aim**

To study the characteristics of current to voltage converter

**Apparatus required**

| | |
|---|---|
| Operational Amplifier μA 741 | - 2 Nos |
| Resistors | |
| Voltmeter (0-10v)mc | - 1 No |
| Ammeter (0-20mA) mc | - 1 No |
| D.C. Dual Power Supply | - 1 No |
| D.C. Power Supply | - 1 No |

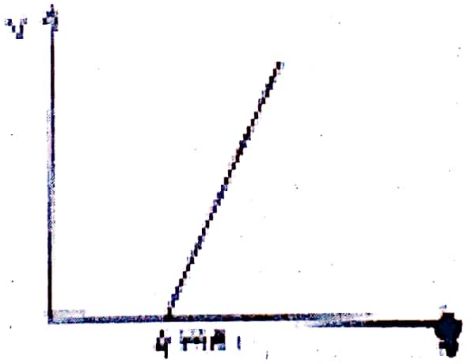
**Specifications**



**Tabular Coloumn**

| I mA | V volts |
|---|---|
| | |

**Model Graph**



**Precautions**

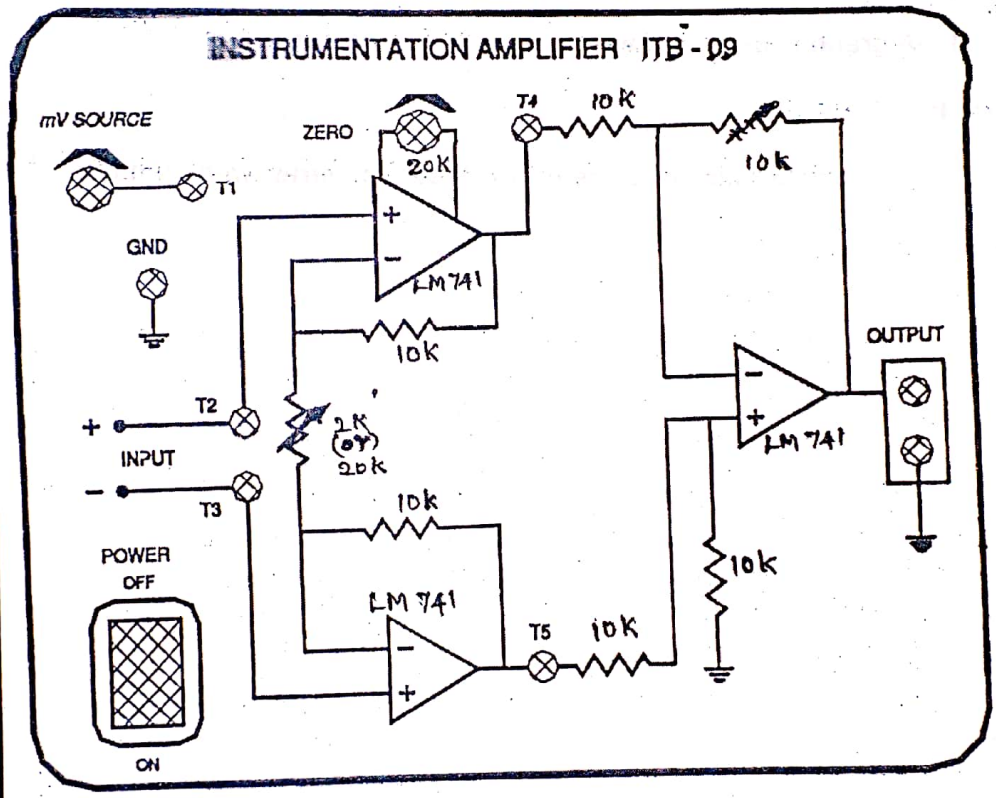
1. The pin numbers should be checked before starting the experiment
2. Loose connections must be avoided.
3. The operational amplifier should be connected with proper polarity and voltage should not exceed $\pm$15 V.

**Procedure**

1. Connections are made as given in the circuit diagram
2. The input voltage is varied from 0 to 10V in steps and the corresponding input currents and output voltages are noted from ammeter and voltmeter respectively
3. A graph is drawn between the voltage and current.

**Result**

Thus characteristics of current to voltage converter was studied.



Expt No:
Date :

## INSTRUMENTATION AMPLIFIER

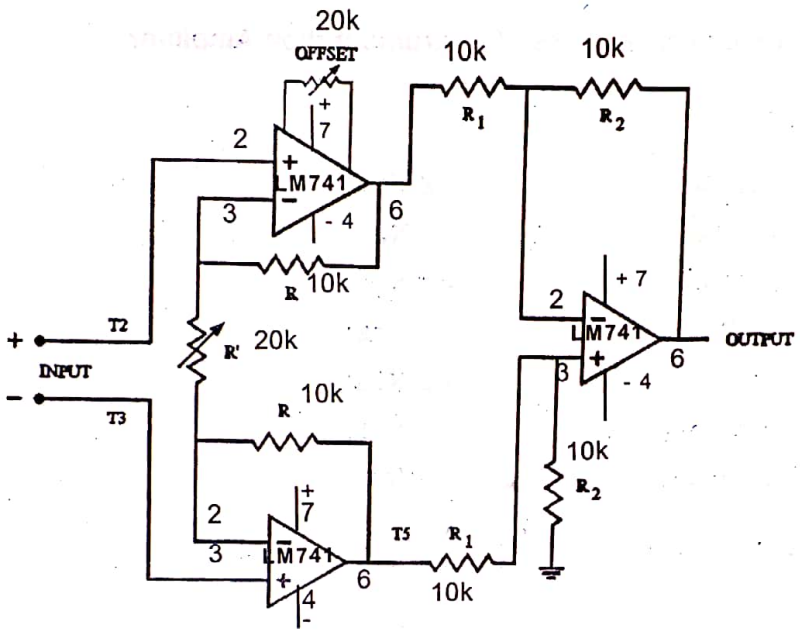
### Aim

To study the characteristics of Instrumentation Amplifier.

### Apparatus required

| | |
|---|---|
| Op- Amp μA 741 | - 2 Nos |
| Resistance 15 kΩ | - 2 Nos |
| 33 kΩ | - 1 No |
| 47 kΩ | - 2 Nos |
| 100 kΩ | - 2 Nos |
| Digital Voltmeter (0-10v) | - 3 Nos |
| Dual Power Supply | - 1 No |

### Specifications




$$Vo = R_2/R_1 (1 + 2R/R') (V_1 - V_2)$$

$R_2 = R_1 = 1K$

$R = 1K$

$R' = \alpha$ for GAIN = 1
= 222E for GAIN = 10
= 22.2E for GAIN = 100

OFFSET = 100K

**Theory**

In analog instrumentation the transducers are frequently located at far distance from the measurement system. The system signal levels at the transducer side are often low and their source impedance are high. A general purpose amplifier for processing such signals is called Instrumentation amplifier.

Instrumentation amplifier should have

1. Differential input
2. High input impedance and CMRR
3. Provided with simple gain adjustment

The instrumentation amplifier is shown in Fig. 1 Operational Amplifiers 1 and 2 are basically connected in non-inverting input configuration. Instead of grounding both the inverting terminals they are connected to resistor $R_2$. The non-inverting terminals at op-amps 1 and 2 are fed by voltage source $V_1$ and $V_2$ respectively.

The voltage at point A is

$$V_A = \left[1 + \frac{R_3}{R_3 + R_4}\right] V_1 - \frac{R_3}{R_3 + R_4} V_B$$

$$= \frac{2R_3 + R_4}{R_3 + R_4} V_1 - \frac{R_3}{R_3 + R_4} V_B$$

## INSTRUMENTATION AMPLIFIER

$T_2$ is +ve w.r.t. $T_3$

**TABULATION**

| $V_2-V_1$(mV) | $V_0$ (mv) | Gain = $\frac{V_0}{(V_2-V_1)}$ | $V_2-V_1$(mV) | $V_0$ (mv) | Gain = $\frac{V_0}{(V_2-V_1)}$ |
|---|---|---|---|---|---|
| | | | | | |

and

$$V_B = \left[1 + \frac{R_3}{R_3 + R_4}\right] V_2 - \frac{R_3}{R_3 + R_4} V_A$$

$$V_{AB} = V_A - V_B$$

$$= \frac{2R_3 + R_4}{R_3 + R_4} (V_1 - V_2) + \frac{R_3}{R_3 + R_4} (V_A - V_B)$$

$$\left[1 - \frac{R_3}{R_3 + R_4}\right] V_{AB} = \frac{2R_3 + R_4}{R_3 + R_4} (V_1 - V_2)$$

$$\frac{R_4}{R_3 + R_4} V_{AB} = \frac{2R_3 + R_4}{R_3 + R_4} (V_1 - V_2)$$

$$V_{AB} = \frac{2R_3 + R_4}{R_4} (V_1 - V_2)$$

$$V_O = \frac{-R_2}{R_1} (V_A - V_B)$$

$$V_O = \frac{-R_2}{R_1} \left[1 + \frac{2R_3}{R_4}\right] (V_1 - V_2)$$

$$= \frac{R_2}{R_1} \left[1 + \frac{2R_3}{R_4}\right] (V_2 - V_1)$$

The overall gain of the two cascaded stage is

$$\frac{V_o}{V_2 - V_1} = \left[1 + \frac{2R_3}{R_4}\right] \frac{R_2}{R_1}$$

The gain may be easily adjusted with out disturbing circuit symmetry by varying the resistance $R_3$.

**Comparison between Instrumentation amplifier and Ordinary amplifier**

1. The instrumentation amplifier consists of two op-amps wired with stable resistance feedback network to give desired gain.
2. Due to closed loop configuration employed, the instrumentation amplifier will often yield high common mode rejection ratio.

## INSTRUMENTATION AMPLIFIER

$T_2$ is -ve w.r.t. $T_3$

### TABULATION

| $V_2$-$V_1$(mV) | $V_0$ (mv) | Gain = $\frac{V_0}{(V_2-V_1)}$ | $V_2$-$V_1$(mV) | $V_0$ (mv) | Gain = $\frac{V_0}{(V_2-V_1)}$ |
|---|---|---|---|---|---|
| | | | | | |

## Precautions

1. The pin numbers should be checked before starting the experiment
2. Loose connections must be avoided.
3. The operational amplifier should be connected with proper polarity and voltage should not exceed $\pm$15 V.

## Procedure

1. The Connections are made as given in the circuit diagram
2. Initially $V_2$ should be kept at 5V and $V_1$ at 0V. Then $V_1$ should be increased from 0V to 5V by keeping $V_2$ constant. The output voltages are noted down using Digital multimeter.
3. Similarly keeping $V_1$ constant at 5V, $V_2$ should be increased from 0V to 5V and the output voltages are noted down.
4. A graph is drawn between $(V_2 - V_1)$ and $V_0$
5. Gain is calculated using the formula

$$\frac{V_0}{V_2 - V_1} = \left[1 + \frac{2R_3}{R_4}\right] \frac{R_2}{R_1}$$

## Result

Thus the characteristics of instrumentation amplifier was studied

Expt No:
Date :

## DESIGN OF LOW PASS FILTERS

**Aim**

To determine the frequency response of first order and second order low pass filters.

**Apparatus required**

| | |
|---|---|
| Op-Amp μA 741 | - 1 No. |
| Digital Voltmeter (0-10v) | - 2 Nos. |
| Dual Power Supply | - 1 No |
| Signal Generator | - 1 No |
| Resistances | |
| Capacitances | |

**Specifications**

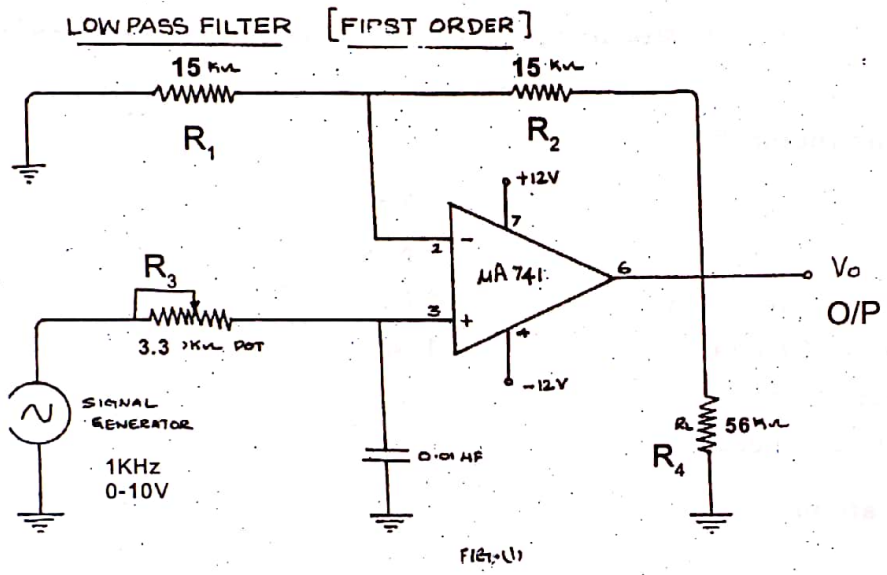
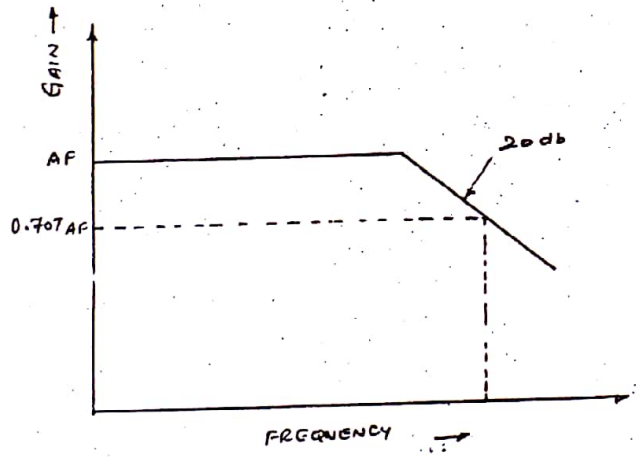



Fig.(1)

## Model waveform



## Theory

Active filters are those which employ transistors and operational amplifiers in addition to resistors and capacitors. The type of elements used decides the operating frequency range of filter. RC filters are commonly used for audio or low frequency operations. LC or crystal filters are employed at RF or at high frequencies.

## First Order Low Pass Butter Worth Filter

Fig. 1 shows a low pass butterworth filter of the first order. As RC network is connected at the non-inverting terminal hence operational will not load it. The purpose of $R_i$ and $R_f$ are to control the gain to the desired level.

The voltage at non-inverting terminal is

$$V_N = \frac{-jX_c}{R-jX_c} V_i$$

$$= \frac{\frac{1}{j\omega C}}{R+\frac{1}{j\omega C}} V_i$$

$$= \frac{V_i}{1+j\omega RC}$$

$$V_0 = \left[1 + \frac{R_f}{R_1}\right] V_N$$

$$V_0 = \left[1 + \frac{R_f}{R_1}\right] \frac{V_i}{1+j\omega RC}$$

$$A = \frac{V_o}{V_i} = \left[1 + \frac{R_f}{R_1}\right] \Big/ 1 + j\omega RC$$

$$A_{max} = \left[1 + \frac{R_f}{R_1}\right]$$

**FIRST ORDER LOW PASS FILTER $V_i$ = .....**

| Frequency in Hz | Output Voltage $V_o$ Volts | Gain db $20 \log \frac{V_o}{V_i}$ |
|---|---|---|
| | | |

At f = $f_{CL}$ (cut off frequency at which gain falls to $\frac{1}{\sqrt{2}}$ of its low frequency value

$$A = \frac{1}{\sqrt{2}} A_{max}$$

$$\frac{1}{\sqrt{2}} A_{max} = \frac{A_{max}}{1+j\omega_{CL}RC}$$

$$f_{cl} = \frac{1}{2\pi RC}$$

$$|A| = \frac{A_{max}}{\sqrt{1+(f / f_{CL})^2}}$$

$$\delta = \arctan (f / f_{CL})$$

If the frequency is made double or increased by 10 times, the gain decreases by 6dB or 20dB, respectively.

**Filter Design**

1. The value of high cut off frequency $f_{CL}$ is chosen as 1 kHz.
2. The value of R is calculated for C = 0.01μF

$$R = \frac{1}{2\pi f_{CL} C} = \frac{1}{2\pi \times 1000 \times 0.01 \times 10^{-6}} = 15.9K\Omega$$

LOW PASS FILTER [SECOND ORDER]

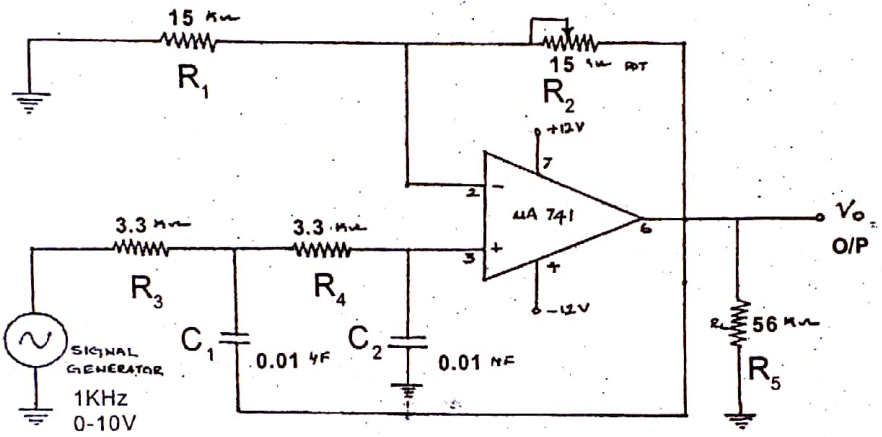
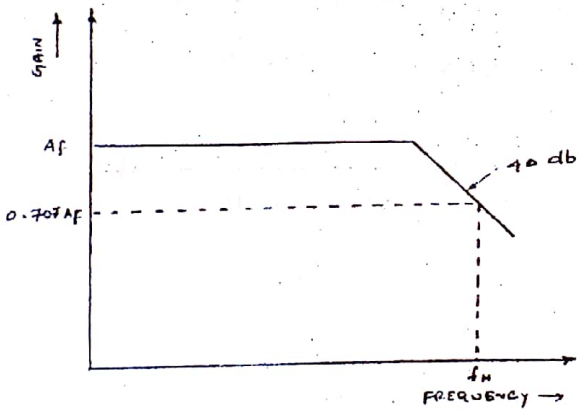



Fig. (iii)

## Model waveform



## Second Order Low Pass Filter

An addition of a RC network converts the first order low pass filter to a 2nd order low pass filter. The response of 2nd order low pass filter is more near to the ideal frequency response. The fall of gain beyond the cut off frequency is -40dB per decade i.e, much sharper than that of 1st order which is -20dB per decade.

The cut off frequency $f_{CL}$ is

$$f_{CL} = \frac{1}{2\pi\sqrt{R_2 R_3 C_2 C_3}}$$

$$A_{max} = 1 + \frac{R_f}{Ri}$$

where $A_{max}$ is the maximum gain and is called the pass gain of the filter.

## Filter Design

1. The value of high cut off frequency $f_{CL}$ is chosen as 1 kHz.
2. Assuming $R_2 = R_3 = R$ and $C_2 = C_3 = C$, the value of R is calculated for

   $C = 0.0047\ \mu F$

$$f_{CL} = \frac{1}{2\pi RC}$$

$$R = \frac{1}{2\pi \times 1000 \times 0.0047 \times 10^{-6}} = 33K\Omega$$

**SECOND ORDER LOW PASS FILTER $V_i$ = .....**

| Frequency in Hz | Output Voltage $V_o$ Volts | Gain db $20 \log \frac{V_o}{V_i}$ |
|---|---|---|
| | | |

**Precautions**

1. The pin numbers should be checked before starting the experiment
2. Loose connections must be avoided.
3. The operational amplifier should be given the proper polarity and voltage should not exceed the limit.

**Procedure**

1. The Connections are made as per the circuit diagram
2. An ac input voltage of 1V is given. Keeping it constant, the frequency is varied from 10 Hz.
3. The output voltage is noted down and the gain 20log $[V_o / V_{in}]$ is calculated.
4. A 3db line is drawn and the cut-off frequency is found. It is compared with the theoretical value.

**Result**

Thus the frequency response of the first order and second order low pass filters were determined.

Expt No:
Date :

## DESIGN OF HIGH PASS FILTERS

**Aim**

To determine the frequency response of first and second order high pass filters.

**Apparatus required**

| | |
|---|---|
| Op-Amp μA 741 | - 1 No. |
| Digital Voltmeter (0-10v) | - 2 Nos. |
| Dual Power Supply | - 1 No |
| Signal Generator | - 1 No |
| Resistances | |
| Capacitances | |

**Specifications**

HIGHPASS FILTER [FIRST ORDER]

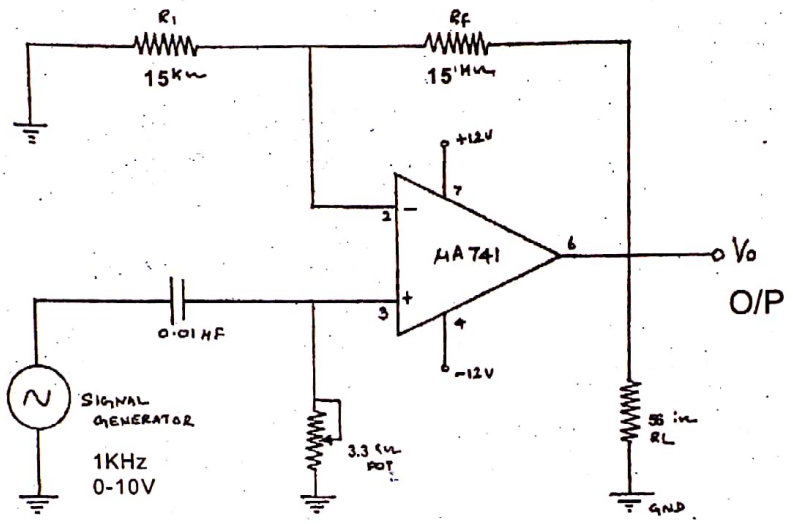
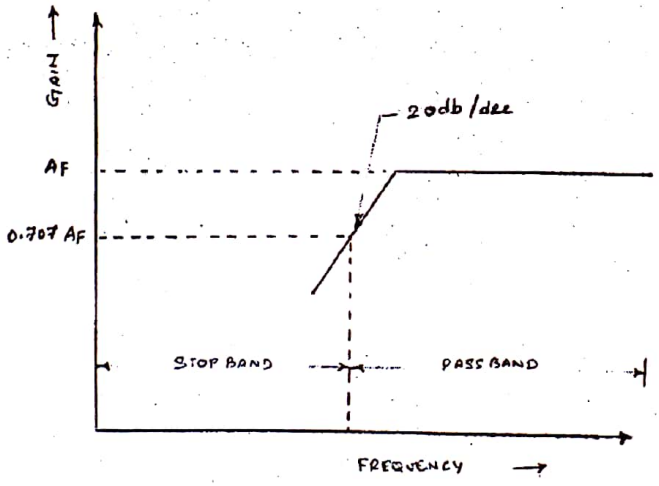



FIG - 1.

## Model waveform



## Theory

Active filters are those which employ transistors and operational amplifiers in addition to resistors and capacitors. The type of elements used decides the operating frequency range of filter. RC filters are commonly used for audio or low frequency operations. LC or crystal filters are employed at RF or at high frequencies.

## First Order High Pass Filter

High pass filters are formed by interchanging components resistors and capacitors in low pass filters. Fig. 1 shows the first order high pass Butterworth filter with cut-off frequency of $f_{CH}$. All frequencies higher than $f_L$ are pass band frequencies.

According to the voltage divider rule, the voltage at the non-inverting terminal is

$$V_N = \frac{V_i}{R + \frac{1}{j\omega C}} \quad R = \frac{j\omega CR}{1 + j\omega CR} \quad V_i$$

$$V_O = \left[1 + \frac{R_f}{R_i}\right] V_N = \left[1 + \frac{R_f}{R_i}\right]\left[\frac{j\omega CR}{1 + j\omega CR}\right] V_i$$

$$A = \frac{V_O}{V_i} = A_{max}\left[\frac{j\omega CR}{1 + j\omega CR}\right]$$

$$A_{max} = \left[1 + \frac{R_f}{R_i}\right]$$

The cut off frequency is the frequency at which the gain is $\frac{1}{\sqrt{2}}$ times the maximum gain $A_{max}$

**FIRST ORDER HIGH PASS FILTER** $V_i$ = .....

| Frequency in Hz | Output Voltage $V_o$ Volts | Gain db $20 \log \frac{V_o}{V_i}$ |
|---|---|---|
| | | |

$$A = \frac{1}{\sqrt{2}} A_{max}$$

$$\frac{1}{2} A_{max} = \frac{A_{max}}{1 - \frac{j}{\omega_{CH} RC}}$$

$$f_{CH} = \frac{1}{2\pi RC}$$

$$|A| = \frac{A_{max}}{\sqrt{1+(f_{CH}/f)^2}}$$

$$\delta = \arctan (f_{CH} / f)$$

$$R = \frac{1}{2\pi f_L C} = \frac{1}{2\pi \times 1000 \times 0.01 \times 10^{-6}} = 15.9K\Omega$$

**Second order High Pass Filter**

Second order High pass filter can be formed from the second order low pass filter simply by interchanging the frequency determining resistors and capacitors.

The voltage gain magnitude is equal to

$$A = \frac{V_o}{V_i} = \frac{A_{max}}{\sqrt{1 + (f_{CH}/f)^2}}$$

**Filter Design**

1. The value of cut off frequency $f_{CH}$ is chosen as 1kHz.
2. Assuming $R_2 = R_3 = R$ and $C_2 = C_3 = C$, the value of R is calculated for C = 0.0047 μF

$$f_{CH} = \frac{1}{2\pi \sqrt{R_2 R_3 C_2 C_3}}$$

HIGH PASS FILTER [SECOND ORDER]

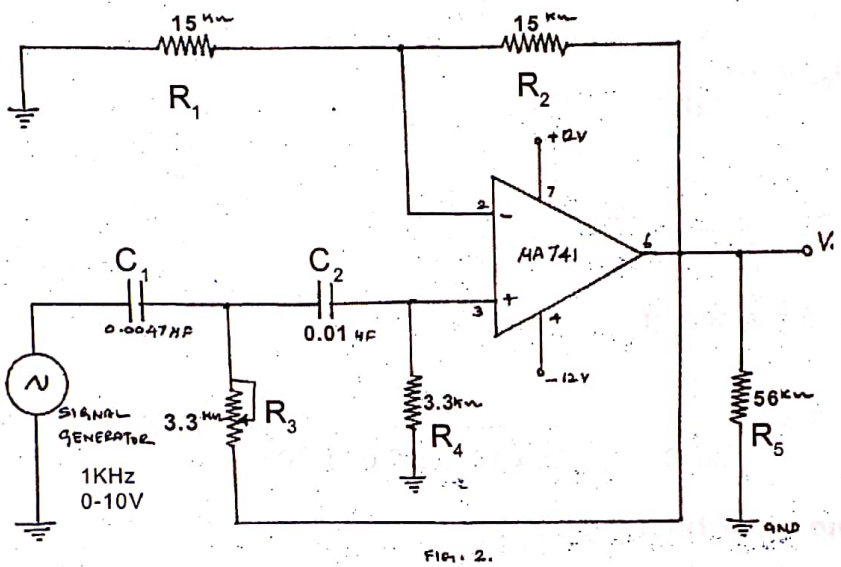
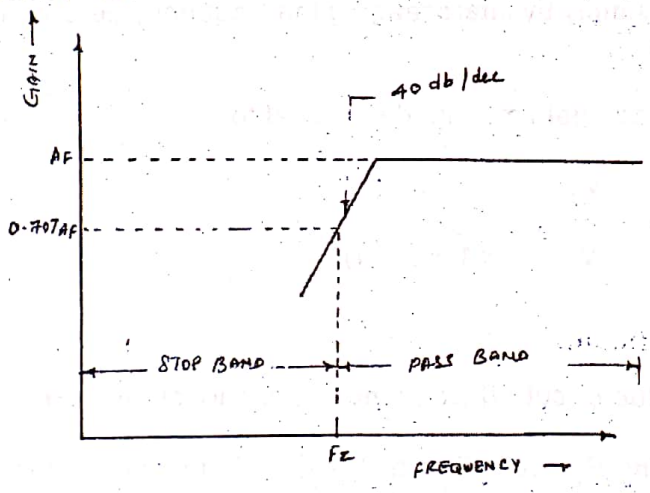



FIG. 2.

**Model waveform**



$$= \frac{1}{2\pi\sqrt{R^2 C^2}}$$

$$= \frac{1}{2\pi RC}$$

$$R = \frac{1}{2\pi \times 1000 \times 0.0047 \times 10^{-6}} = 33K\Omega$$

**Precautions**

1. The pin numbers should be checked before starting the experiment.
2. Loose connections must be avoided.
3. The operational amplifier should be given the proper polarity and voltage should not exceed the limit.

**Procedure**

1. The connections are made as per the circuit diagram.
2. An ac input voltage of 1 V is given. Keeping it constant, the frequency is varied from 10Hz.
3. The output voltage is noted down and the gain $20\log (V_o / V_{in})$ is calculated.
4. A 3dB line is drawn and the cut-off frequency is found. It is compared with the theoretical value.

**Result**

Thus the frequency response of the first order and second order high pass filters were determined.

**SECOND ORDER HIGH PASS FILTER $V_i$ = .....**

| Frequency in Hz | Output Voltage $V_o$ Volts | Gain db $20 \log \frac{V_o}{V_i}$ |
|---|---|---|
| | | |